**Code:**

* **Design Module**
* **2x1 Module**

// Code your design here

// mux 2x1

module Mux\_2x1(input wire in1, // ports

input wire in2,

input wire sel,

output reg out);

wire out\_val; //temp singal - internal wire

assign out\_val = (sel)? in2:in1; // mux logic

always@(\*) //sensitivity list for record change at change of specified signal

begin

out <= out\_val ; // tieing temp output signal (internal wire to output register)

end

endmodule

* **Main Design Module**

// Code your design here

// mux 8x1

`include"Mux\_2x1.sv"

module Mux\_8x1(input in1,

input in2,

input in3,

input in4,

input in5,

input in6,

input in7,

input in8,

input sel\_a,

input sel\_b,

input sel\_c,

output out); //ports

wire temp\_1,temp\_2,temp\_3,temp\_4,temp\_5,temp\_6;//internal wires

Mux\_2x1 mux1(in1,in2,sel\_c,temp\_1);

Mux\_2x1 mux2(in3,in4,sel\_c,temp\_2);

Mux\_2x1 mux3(in5,in6,sel\_c,temp\_3);

Mux\_2x1 mux4(in7,in8,sel\_c,temp\_4);

Mux\_2x1 mux5(temp\_1,temp\_2,sel\_b,temp\_5);

Mux\_2x1 mux6(temp\_3,temp\_4,sel\_b,temp\_6);

Mux\_2x1 mux7(temp\_5,temp\_6,sel\_a,out);

endmodule

* **TestBench**

// Code your testbench here

// or browse Examples

module tb();

reg input\_1,input\_2,input\_3,input\_4,input\_5,input\_6,input\_7,input\_8;

reg select\_a,select\_b,select\_c;

wire result;

// Mux\_8x1 tb\_1(input\_1),.in2(input\_2),.in3(input\_3),.in4(input\_4),.in5(input\_5),.in6(input\_6),

// .in7(input\_7).in8(input\_8),.sel\_a(select\_a),.sel\_b(select\_b),.sel\_c(select\_c),

// .out(result));

Mux\_8x1 tb\_1(input\_1,input\_2,input\_3,input\_4,input\_5,input\_6,input\_7,input\_8,select\_a,select\_b,select\_c,result);

initial

begin

input\_1 = $random;

input\_2 = $random;

input\_3 = $random;

input\_4 = $random;

input\_5 = $random;

input\_6 = $random;

input\_7 = $random;

input\_8 = $random;

#10

select\_a = 1'b0;select\_b = 1'b0;select\_c = 1'b0;

#10

select\_a = 1'b0;select\_b = 1'b0;select\_c = 1'b1;

#10

select\_a = 1'b0;select\_b = 1'b1;select\_c = 1'b0;

#10

select\_a = 1'b1;select\_b = 1'b0;select\_c = 1'b0;

#10

select\_a = 1'b1;select\_b = 1'b0;select\_c = 1'b1;

end

// only for waveforms on eda playground

// initial

// begin

// $dumpfile("dump.vcd");

// $dumpvars();

// #60

// $finish;

// end

endmodule

**Output:**

A screenshot of a computer

Description automatically generated with medium confidence